

A 1.8 TO 4 GHZ RECEIVER FRONT-END WITH 250 MHZ BASEBAND BANDWIDTH FOR ADVANCED CELLULAR APPLICATIONS

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ARTICLE INFO	ABSTRACT
Received: 27/12/2021	This paper presents a wide-band inductor-less receiver front-end with wide baseband bandwidth. A direct conversion receiver based on this structure is appropriate for a fifth-generation (5G) receiver or other wireless systems. The broadband receiver front-end includes a low-noise amplifier (LNA), a passive mixer, and a wide-band transimpedance amplifier (TIA). The LNA employs a complementary current-reuse common source amplifier combined with a low-current active feedback to achieve simultaneously low noise and high linearity. A current-reuse self-biasing TIA is proposed to obtain wide-band and quite-linear. The proposed receiver front-end is implemented in 28 nm CMOS process. It has a RF bandwidth of 2.2 GHz and a baseband bandwidth (BBBW) of 250 MHz. The noise figure (NF) is 5.5 dB and the conversion gain is larger than 15.9 dB with passband variations under 0.7 dB in BBBW of 250 MHz. The third-order input intercept point (IIP3) is 3 dBm at 2.3 GHz, whereas it consumes 75.2 mW at a 0.9-V supply and has an area of 0.053 mm ² .
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THIẾT KẾ MẠCH FRONT-END TRONG MÁY THU TỪ 1.8 ĐẾN 4 GHZ VỚI BĂNG THÔNG BĂNG GỐC 250-MHZ CHO CÁC ỨNG DỤNG DI ĐỘNG TẾ BÀO THỂ HỆ MỚI

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THÔNG TIN BÀI BÁO	TÓM TẮT
Ngày nhận bài: 27/12/2021	Bài báo này trình bày về mạch cao tần không sử dụng cuộn cảm với băng thông băng gốc rộng trong máy thu băng rộng. Máy thu chuyển đổi trực tiếp dựa trên cấu trúc này thích hợp cho máy thu 5G hoặc các hệ thống không dây khác. Mạch cao tần trong máy thu băng rộng bao gồm mạch khuếch đại tạp âm thấp (LNA), mạch trộn tần thụ động và mạch khuếch đại biến đổi dòng-áp dải rộng (TIA). LNA sử dụng cấu trúc mạch khuếch đại nguồn chung tái sử dụng dòng kết hợp với mạch phản hồi tích cực dòng thấp để đạt được đồng thời cả tạp âm thấp và độ tuyến tính cao. Mạch TIA tự phân áp tái sử dụng dòng được đề xuất để đạt được băng thông rộng và độ tuyến tính cao. Mạch cao tần trong máy thu đề xuất được thiết kế trên công nghệ CMOS 28 nm. Mạch có băng thông RF là 2,2 GHz và băng thông băng gốc (BBBW) là 250 MHz. Hệ số tạp âm (NF) là 5,5 dB và độ lợi chuyển đổi điện áp lớn hơn 15,9 dB với khoảng thay đổi độ lợi nhỏ hơn 0,7 dB trong BBBW 250 MHz. Điểm chặn đầu vào bậc ba (IIP3) là 3 dBm tại tần số 2,3 GHz. Mạch tiêu thụ 75,2 mW với nguồn cung cấp 0,9 V và có diện tích chiếm là 0,053 mm ² .
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TỪ KHÓA	
Máy thu chuyển đổi trực tiếp	
Băng thông băng gốc rộng	
Ứng dụng di động tế bào	
Khuếch đại tạp âm thấp dải rộng	
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1. Introduction

In recent years, a high data-rate has become significantly demanded aspects in some mobile applications such as software defined radio and high performance cellular applications. The easiest way to obtain this goal is to use larger channel bandwidths, as it was done in third-generation mobile communication systems (3G) and long-term evolution (LTE). 5G working in the sub-6 GHz frequency band requires a signal bandwidth of 200 MHz or higher [1]. This is a challenge in direct conversion receiver front-end design. In addition, the receivers need to deal with large out-of-band (OOB) blockers (a strong interferer), while frequency-division duplex also introduces strong self-interference from the transmitter. To prevent degradation in sensitivity, a off-chip high-linearity surface acoustic-wave (SAW) filters are often adopted [2]. However, these filters increase size and cost, and introduce 2–3 dB of in-band loss. As a result, SAW-less solutions compatible with CMOS integration are highly desired. Several solutions to this problem were presented in [3]–[9], based on the mixer-first receiver architecture. Reference [3] employs two passive-mixer-based down conversion paths to enhanced the receiver's tolerance to harmonic blockers. References [4], [5] use passive switch-capacitor N-path filters with tunable center frequency to obtain more 10-dBm blocker 1-dB compression point and a good input-referred third-order intercept point (IIP3) of 20–30 dBm. In [6], $g_m C$ filter technique is implemented to achieve good selectivity. In [7], a highly linear N-path filter with bottom-plate sampling implements OOB filtering at RF to improve IIP3 and compression. In [8], a baseband impedance with a 40 dB/decade roll-off using positive feedback is generated to enhanced selectivity. By presenting an impedance that rolls off at 40 dB/decade as the load to an N-path filter, receiver in [9] improves channel selectivity, linearity in the presence of OOB blockers. While achieving extremely high linearity for far away blockers, these receivers have baseband bandwidth (BBBW) less 10 MHz. Thus, it is difficult for mixer-first architecture to achieve simultaneous wide BBBW and high linearity. To overcome this issue, the receiver architecture based on low noise amplifier (LNA), mixer and TIA has been introduced in [10], [11]. In [10], a baseband noise-canceling topology and an inverter-based amplifier architecture are implemented to achieve 175 MHz of BBBW and 9 dBm of IIP3. In [11], a common-gate-based transconductance amplifier with cross-coupled structure and resistive degeneration and a wide-band TIA are employed to obtain 200 MHz of BBBW and 15.1 dBm of IIP3. However, reference [10] has high power dissipation of 172 mW and [11] uses inductors in LNA.

This paper proposes a wide-band inductor-less receiver front-end architecture. By using a LNA with combining of complementary current-reuse common source amplifier and low-current active feedback and a current-reuse self-biasing wide-band TIA, the proposed receiver front-end achieves high linearity and wide BBBW simultaneously. In addition, the design process of LNA, Mixer and TIA is adopted. This paper is organized as follows. Section 2 introduces the architecture of the proposed receiver. Next, in Section 3, the circuit implementation is described in detail. Section 4 provides the experimental results on 28 nm CMOS process followed by conclusions in Section 5.

2. Receiver Front-End Architecture

A common situation in receiver front-end design is that the receiver senses a weak desired signal along with a blocker. When the blocker travels through the receive chain, it is amplified and can introduce significant distortion. Therefore the chain must be designed for sufficient linearity up to the stage where the blocker is filtered. As a result, the linearity is a considerable target in receiver front-end design. In addition, for advanced cellular applications, wide BBBW is necessary to achieve high speed. To obtain both wide BBBW and high linearity requirements, we proposes a receiver front-end architecture as shown in Figure 1. It consists of a wide-band LNA, a current-driven passive mixer and a wide-band TIA instead of mixer-first architecture.

As depicted in Figure 1, capacitors C_{in} and C_{out} are used to block DC for the input and output of the receiver front-end, respectively. Five digital control bits (B0-B4) are used to select the degeneration resistor value (see R_D in Figure 2) in the LNA circuit to achieve a high linearity under influence of process, voltage and temperature. Capacitor C_1 plays two roles: DC block and matching between the output of LNA and the input of mixer. Feedback resistor R_{F1} is used to convert current at the output of mixer to voltage for baseband and bias for the TIA. Capacitors C_2 and C_F help to filter blocker. Furthermore, C_F adds a zero in the feedback path to improve the stability of the TIA.

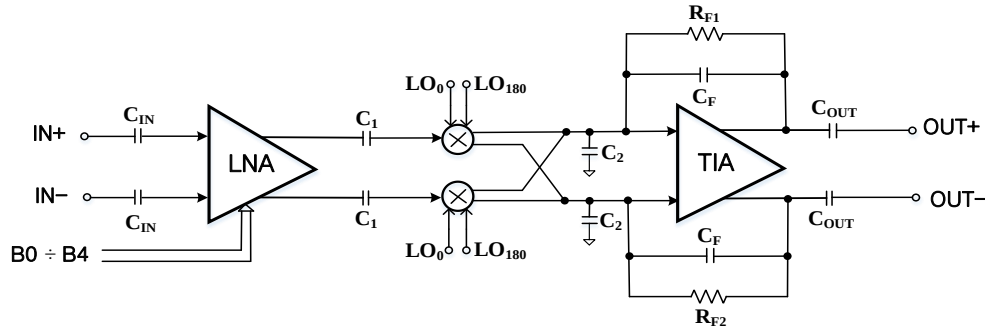


Figure 1. The block diagram of proposed receiver front-end

3. Circuit Implementation

3.1. Wide-band inductor-less highly linear LNA

A wide-band, low noise, and high linear receiver requires a wide-band, low noise, and high linearity LNA circuit. In addition, to fall area in this work we proposes an inductor-less LNA as shown in Figure 2 [12], [13]. It consists of a main amplifier (A) and a shunt feedback path (F). The main amplifier bases on a current-reuse structure with PMOS and NMOS pairs (M1, M2) connected in series. The R_B resistor is used to bias for M1, M2. The current-reuse structure boosts transconductance so the LNA obtains low NF and high gain simultaneously [10]. The active feedback loop employs source follower structure to enable a wide-band matching and a high linearity of the LNA. A degeneration resistor (R_D) is added to enhance linearity of the LNA. To counter the effects of process, voltage and temperature, R_D is adjusted to change feedback current (I_{FB}). In this work, we use five digital control bits (B0÷B4) to create 32 degeneration resistance values. As a result, the LNA will achieve a wide range of the IIP3.

Based on the circuit analysis that was performed in [12], [13]: the gain of the LNA is decided by G_m of stage A; By optimizing the gain and feedback resistor (R_F) wide-band input impedance matching could obtain; Transistors M1, M2 and bias resistor R_B are main noise distribution of the LNA, a design process for the proposed LNA is presented as follows.

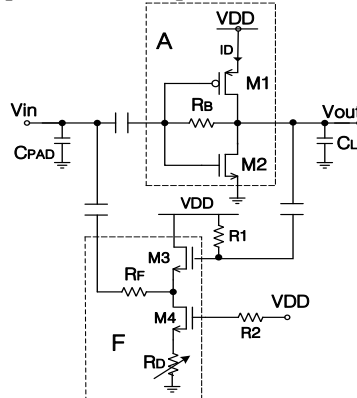


Figure 2. Circuit detail of wide-band LNA

Step 1: The block A is designed with a large G_m to meet gain and NF of the LNA (the width of M1 and M2 is chosen large). Moreover, R_B must also be selected large enough to ensure gain and minimize its noise contribution to the overall circuit noise.

Step 2: Design block F. Firstly, R_D is selected to generate I_{FB} of 1 mA to save power. The size of M3, M4 is designed enough large to decrease noise from the block F to the whole circuit. Then, select R_F value to meet the wide-band input impedance matching. R_F impacts both gain and input impedance matching so it must be swept to select the optimal value.

Step 3: Change I_{FB} to meet IIP3. After that, check again the input impedance matching to make an optimal value of the I_{FB} .

Table 1 illustrates the parameters in the LNA circuit after following the steps in the LNA design.

Table 1. Design parameter values in the LNA (in CMOS 28 nm)

M1	180 μ m/30 μ m	M2	180 μ m/30 μ m	M3	60 μ m/30 μ m
M4	60 μ m/30 μ m	R_B	4.5 k Ω	R_F	240 Ω

In this work, I_{FB} is designed from 40 μ A to 1.28 mA with a linear gain of 40 μ A (32 possible values of the I_{FB} are made by 5 digital control bits (B0÷B4)). The smaller the resolution of the I_{FB} , the better the IIP3 with a little trade-off of power and area.

3.2. Passive Mixer

In a zero-IF receiver any flicker noise in its down-conversion mixer appears in the signal band of interest. In the conventional Gilbert-type active mixer the switches steer the RF signal together with the bias current [14]. Additionally, due to current-to-voltage followed by voltage-to-current conversions, the combined LNA and active mixer suffers from poor linearity and is generally not sufficient for today's multi-band receivers. To overcome this problem, the current-driven passive mixer was proposed in [15] and nowadays this mixer is already commonly used in receivers. RF current is passed to mixer whose switches are clocked by clocks (LO). There are two types of driven clock: rail-to-rail 25% duty-cycle and rail-to-rail 50% duty-cycle. Where a passive mixer driven by a 25% duty-cycle LO has better linearity and 3 dB higher conversion gain than driven by a 50% duty-cycle LO [16], [17]. Therefore, in this work, we propose to use the 25% duty-cycle LO to drive mixer as shown in Figure 3. The mixer includes four NMOSs where are driven by 25% duty-cycle LOs (LO_0 and LO_{180}).

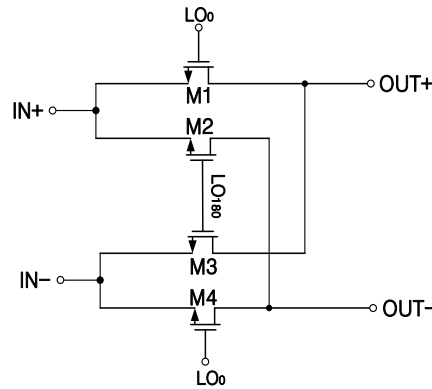


Figure 3. Circuit detail of current-driven passive mixer

The performance of the mixer is inversely proportional to the open resistance (R_{on}) of the switches (M1, M2, M3, M4 in Figure 3) [16]. Figure 4 shown relationship between R_{on} and size of switches. R_{on} decreases when the size of switches increase. Thus, the size of switch is selected as 160 μ m to minimum R_{on} ($R_{on} = 4 \Omega$) and save area as well.

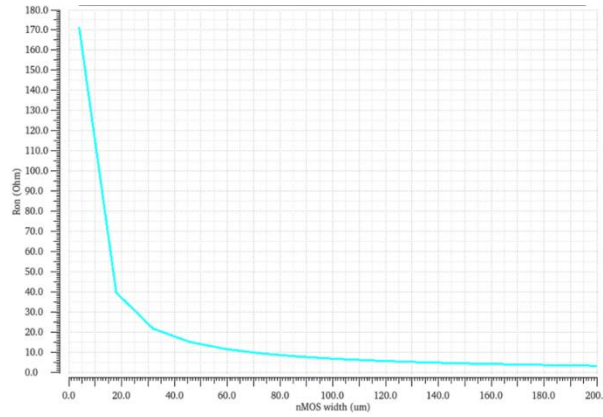


Figure 4. Relationship between R_{on} and size of switches

3.3. Wide-band low-noise TIA

A CMOS inverter with a large G_m is a good candidate to make a low-noise quite-linear TIA [10]. However, this structure is pseudo differential so it needs extra circuitry to decrease the common mode gain, while maximizing differential mode gain. Consequence, it often leads to extra power dissipation and noise (172 mW in [10]). Therefore, in this work, we propose a TIA architecture with a low common mode output impedance by using M1P and M2P which are put above the inverters (M3P, M1N and M4P, M2N) for current-reuse as shown in Figure 5. The inverters are biased by R_{F1} and R_{F2} (see Figure 1). The current sources are generated by M1P and M2P to ensure that four transistors below operate in sub-threshold region. This helps to enhance linearity of the TIA and save power as well. There are four important criteria in TIA circuit design: linearity, noise, BBBW and DC gain. In which, the linearity and noise are decided by G_m of inverter. The BBBW and DC gain depends on feedback resistor (R_{F1} , R_{F2}). While the BBBW is inversely proportional to the feedback resistance, the DC gain is directly proportional to the feedback resistance. In addition, the DC gain is also inversely proportional to the G_m of inverter and the linearity is affected by the feedback capacitor (C_F). Thus, we see that there is a trade-off between DC gain and linearity and BBBW. With the goal of designing a receiver front-end with high linearity and wide BBBW, the DC gain criterion can be loosened in the design. We can compensate for low DC gain of TIA by increasing gain of LNA or BB circuit in receiver chain. Based on the above analysis, a TIA design process is presented as follows.

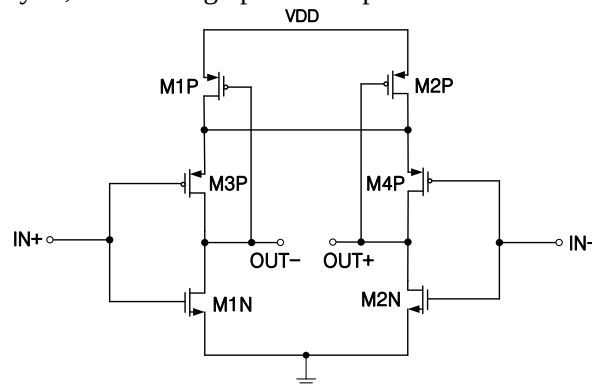


Figure 5. Circuit detail of proposed TIA

Step 1: Design inverter with large G_m to meet requirements of noise and linearity. Check operating point of M3P, M1N, M4P, M2N to ensure they operate in sub-threshold region.

Step 2: Sweep C_F to achieve the linearity and choose optimal C_F value.

Step 3: Reduce R_{F1} , R_{F2} to extend BBBW until it reaches to target.

Step 4: Check linearity, noise and DC gain again, If they do not satisfy the requirements, perform an R_{F1} , R_{F2} sweep to find the optimal R_{F1} , R_{F2} value.

After following the steps in the TIA design, we obtain the values of the parameters in the TIA circuit as presented in Table 2.

Table 2. Design parameter values in the TIA

M1P	75 $\mu\text{m}/30 \mu\text{m}$	M2P	75 $\mu\text{m}/30 \mu\text{m}$	M3P	4620 $\mu\text{m}/30 \mu\text{m}$	R_{F1}	40 Ω
M4P	4620 $\mu\text{m}/30 \mu\text{m}$	M1N	2310 $\mu\text{m}/30 \mu\text{m}$	M2N	2310 $\mu\text{m}/30 \mu\text{m}$	C_F	200 fF

4. Simulation Results and Discussion

A 1.8 to 4 GHz receiver front-end is designed based on the above analysis. The proposed inductor-less receiver front-end is implemented in a 28 nm CMOS process. Figure 6 shows the layout picture of the receiver front-end. It occupies 284 μm x 186 μm core silicon area without the Pads. The power dissipation is 75.2 mW from a 0.9 V supply voltage (The LNA consumes 33.4 mW and Mixer and TIA consume 41.8 mW).

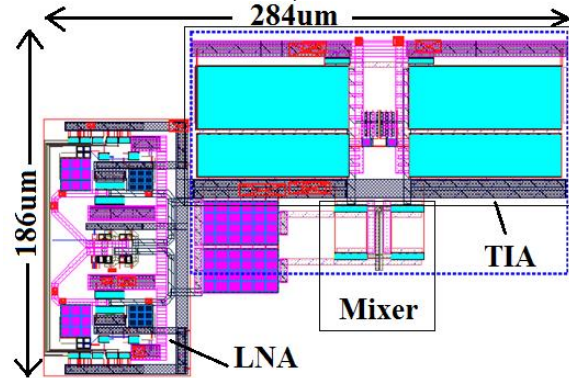


Figure 6. Layout of receiver front-end

The post-layout simulation of the receiver front-end is illustrated from Figure 7 to Figure 10. The simulated input match is shown in Figure 7 (the input impedance is set to 50 Ω). The input reflection coefficient (S_{11}) is better than -11.5 dB from 1.8 to 4.2 GHz. This result demonstrates that the receiver front-end achieves wide-band operation. The receiver front-end obtains conversion gain higher than 15.9 dB with less than 0.75 dB gain ripple over the BBBW of 250 MHz (see Figure 8). With the achieved flatness of gain and wide BBBW, the proposed receiver front-end can be used in advanced cellular applications. The simulated NF is depicted in Figure 9. The NF at 1 MHz and the flicker frequency are approximately 5.53 dB and 40 kHz, respectively. The low flicker frequency achieved makes this architecture suitable for direct conversion receivers.

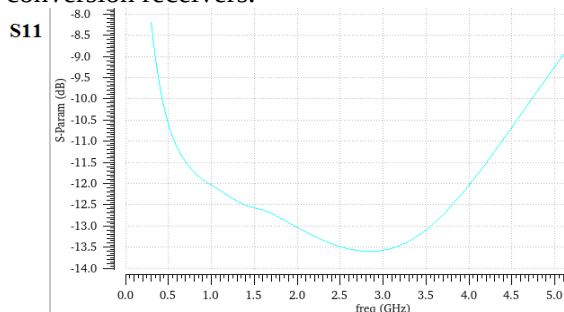


Figure 7. Simulated S_{11} at LNA input versus input frequency

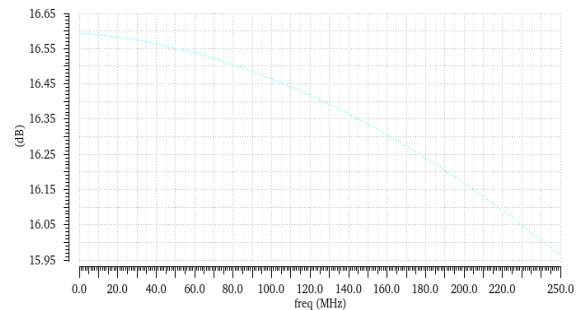


Figure 8. Simulated conversion gain of receiver front-end versus BBBW

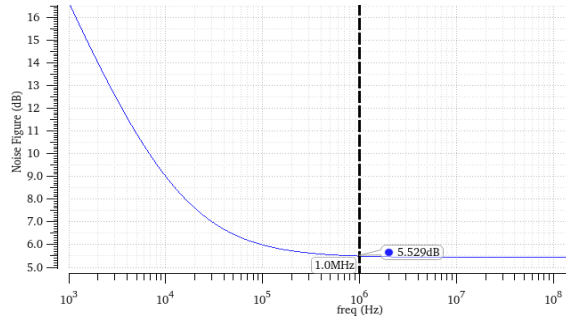


Figure 9. Simulated NF of receiver front-end

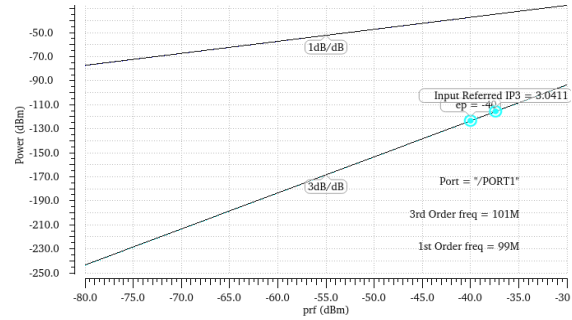


Figure 10. Simulated IIP3 of receiver front-end

Linearity is simulated with a three-tone test: 2.4 GHz, 2.3 GHz and 2.301 GHz. The post-layout simulation of IIP3 is demonstrated in Figure 10. The simulated IIP3 is 3 dBm. In this work, a post-layout simulation of IIP2 is also realized. This receiver front-end has the simulated IIP2 of 58.7 dBm. These are competitive numbers in addition to the wide-band frequency of operation and the wide BBBW of the receiver front-end. Table 3 lists a summary of CMOS receiver front-ends in literature. This work has the widest BBBW and comparable conversion gain, NF, IIP3 when compared to [9]-[11]. Reference [11] achieves the BBBW of 200 MHz and a highest IIP3 of 15.1 dBm but it uses inductors in the LNA so it has a biggest area of 1.23 mm².

Table 3. Performance Comparison of LNA

	[9] (measure)	[10] (measure)	[11] (measure)	This work (post-simulation)
Technology	28nm CMOS	22nm FDSOI	40nm CMOS	28nm CMOS
Supply (V)	1.2	0.83	1.1	0.9
Architecture	Mixer-first RX	LNA+Mixer+TIA	LNA+Mixer+TIA	LNA+Mixer+TIA
RF BW (GHz)	1.8	5	3	2.2
BB BW (MHz)	9	175	200	250
Inductor	No	No	Yes	No
Conversion gain (dB)	14.5	22	13	15.9
NF (dB)	7.6	5	5.8	5.5
IIP3 (dBm)	5	9	15.1	3
Area (mm ²)	0.48	0.48	1.23	0.053
Power (mW)	143	172	69.6	75.2

5. Conclusion

The proposed inductor-less receiver front-end is implemented in 28 nm CMOS process. The receiver front-end achieves wide-band, small gain variation across the working bandwidth, wide-baseband bandwidth and high linearity by combining a wide-band, low-noise, high linearity LNA, a passive mixer driven by 25% duty-cycle LO and a wide-band TIA. A current-reuse self-biasing TIA is employed to enhance BBBW to 250 MHz in post-layout simulation, outperforming previous published receiver front-end. The limitation of this work is that there are no measurement results yet. Therefore, in future work, we will tape out chip to get measured results and keep researching to further improve the linearity of the receiver front-end.

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