# A 2.4 TO 3 Gb/s REFERENCE-LESS HALF-RATE CDR WITH ADAPTIVE EQUALIZER IN WIRELINE RECEIVERS

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**ABSTRACT**

This paper presents a 2.4 to 3 Gb/s reference-less half-rate clock and data recovery (CDR) with combined adaptive equalizer (EQ) in wireline receiver. A wide-band receiver based on this structure is appropriate for a high-speed wireline systems. The broadband CDR achieves by using a two-step frequency tracking scheme: coarse and fine. In addition, in this work the coarse/fine frequency acquisition processes operate simultaneously to obtain a fast frequency acquisition time. The adative continuous-time linear equalizer (CTLE) based on sampled data edge counting is employed to achieve both short adaptive time and low power dissipation. A combination of EQ and CDR is proposed to achieve fast data recovery and processing times for the receiver. The proposed receiver is implemented in 180 nm CMOS process. It has the adaptive time of 4.4 µs and a frequency acquisition time of 3 µs for the tracking range from minimum frequency to maximum frequency of the voltage controlled oscillator (VCO). The receiver circuit has shown peak-to-peak jitter in recovered clock and data of 40 ps and 70 ps, respectively, with 3 Gb/s input data, whereas it consumes 42.7 mW at a 1.8-V supply.

# THIẾT KẾ MẠCH CDR BÁN TỐC KHÔNG SỬ DỤNG TẦN SỐ THAM CHIẾU TỪ 2.4 ĐẾN 3 Gb/s KẾT HỢP VỚI MẠCH SAN BẰNG THÍCH NGHI TRONG MÁY THU CÓ DÂY

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**TỪ KHÓA**

Máy thu có dây tốc độ cao
Không sử dụng tần số tham chiếu
Mạch khôi phục dữ liệu và xung đồng hồ
Mạch san bằng thích nghi
Thời gian bám tần số ngắn

**TÓM TẮT**

Bài báo này trình bày về mạch khôi phục dữ liệu và xung đồng hồ (CDR) bán tốc không sử dụng tần số tham chiếu từ 2,4 đến 3 Gb/s kết hợp với mạch san bằng thích nghi trong máy thu có dây. Máy thu băng rộng dựa trên cấu trúc này thích hợp cho các hệ thống có dây tốc độ cao. Mạch CDR băng rộng đạt được bằng cách sử dụng sơ đồ bám tần số theo hai bước: thô và tinh. Ngoài ra, trong nghiên cứu này, quá trình bám tần số thô và tinh hoạt động đồng thời để đạt được thời gian bám tần số ngắn. Mạch san bằng tuyến tính thời gian liên tục (CTLE) dựa trên bộ đếm được sử dụng để đạt được đồng thời cả thời gian thích nghi ngắn và công suất tiêu thụ thấp. Sự kết hợp giữa CDR và EQ được đề xuất để đạt được thời gian xử lý và khôi phục dữ liệu nhanh cho máy thu. Máy thu đề xuất được thiết kế trên công nghệ CMOS 180 nm. Mạch có thời gian thích nghi là 4,4 µs và thời gian bám tần số là 3 µs với khoảng bám từ tần số nhỏ nhất đến tần số lớn nhất của bộ dao động điều khiển bằng điện áp (VCO). Máy thu có jitter của xung đồng hồ và dữ liệu khôi phục lần lượt là 40 ps và 70 ps với dữ liệu đầu vào là 3 Gb/s. Mạch tiêu thụ công suất 42,7 mW với nguồn cung cấp 1,8 V.

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## 1. Introduction

In serial data communication systems, a clock and data recovery (CDR) circuit is placed at the receiver side to recover the data from an incoming data stream and should run at the high rate. CDRs can be classified as referenced or reference-less. The first method uses an external reference clock for frequency acquisition. This method is simple but it increases the design cost. The second method extracts directly the clock from the input data stream without an external reference clock. Thereby, it can be used for many different applications. Recently, the reference-less CDRs are widely adopted in various applications [1] – [5]. However, frequency acquisition methods in [1], [2] use a unilateral frequency detector (FD), in which, [1] and [2] suggested initiating the operation of voltage controlled oscillator (VCO) from the minimum and maximum frequency for frequency tracking process, respectively. This leads to a longer frequency acquisition time. To overcome limitation of the unilateral FD, the several bidirectional FDs in the CDR designs were proposed [3] - [5]. A uniform probability of 0.25 for all four possible transitions of the random data patterns was assumed in [3]. Consequence, the CDR performance strongly depended on transition density of the input data. In [4], the frequency acquisition process always starts from the middle band of the VCO, resulting in longer frequency acquisition time of the CDR circuit. The counter-based FD [5] is employed to obtain unrestricted frequency acquisition in reference-less CDR but its performance also could be degraded by the inter-symbol interference (ISI).

The demand for a higher data bandwidth in serial data communication keeps increasing with respect to the development of CMOS technology performance. To meet this requirement while ensuring low bit error rate (BER), the equalizers (EQ) at the receiver side are used because of the poor channel conditions at higher data rates. However, because channel conditions are not always known in advance for data transmission, an EQ circuit with a pre-designed channel loss compensation factor does not achieve optimal equalization performance. Thus, adaptive EQ circuits become more relevant in practice and more attractive in research [6] – [10]. In [6], the spectrum balancing technique has been used for continuous-time linear equalizer (CTLE) adaptation process. However, it suffers from process, voltage, and temperature (PVT) variations. The adaptation method based on the slope-detection for the CTLE is presented in [7] but it requires large power dissipation. Design [8] illustrates the adaptive equalization method based on an eye-opening monitor. However, the quality of the EQ is strongly dependent on the transfer density of the input data. To overcome these drawbacks, counter-based adaptive techniques are proposed in [9], [10]. However, these EQs require an external reference clock to generate the time windows and to sample the data.

In high-speed wireline receivers, a CDR circuit is combined with an EQ to achieve low BER [11] – [15]. However, the receivers in [11] – [13] employed an external reference clock for frequency acquisition process. The receiver architectures in [14], [15] is reference-less but they had a long frequency tracking time, 680 μs in [15] and 5.5 ms in [14]. Moreover, the equalizers in [14], [15] do not have the ability to adapt to different channel conditions.

This paper proposes a receiver architecture including an adaptive EQ and a reference-less CDR. By using an adaptive EQ based on counter [16] and a CDR with two-step frequency tracking scheme [17], the proposed receiver achieves short adaptation and frequency tracking time, and a reasonable power consumption, simultaneously. This paper is organized as follows. Section 2 introduces the architecture of the proposed receiver. Next, in Section 3, the principle of the adaptive equalization and frequency detection in wireline receiver is described in detail. Section 4 shows the experimental results on 180 nm CMOS process followed by conclusions in Section 5.

## 2. Receiver Architecture

Figure 1 illustrates the block diagram of the proposed half-rate wireline receiver circuit. It consists of an adaptive EQ, a current mode logic (CML)-to-CMOS circuit and a reference-less

CDR. After the adaptive EQ, the data is fed into the CML-TO-CMOS circuit to convert to full-swing data for the CDR. The CDR includes a half-rate bang-bang phase detector in current-mode logic for high speed, a wide-band frequency detector, a VCO and two charge pump circuits. In this dual-loop CDR circuit, both frequency detector and phase detector use the same loop filter via the connection of switches S1 and S2, respectively. Switch S1 selects the frequency locked loop and switch S2 selects the phase locked loop. The FD comprises a coarse FD, a fine FD and a frequency lock detector. A decision circuit is utilized to recover data.

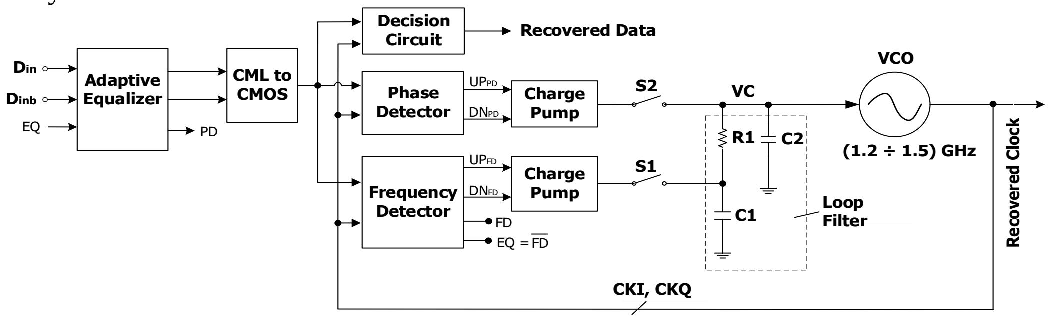



**Figure 1.** *The block diagram of proposed wireline receiver*

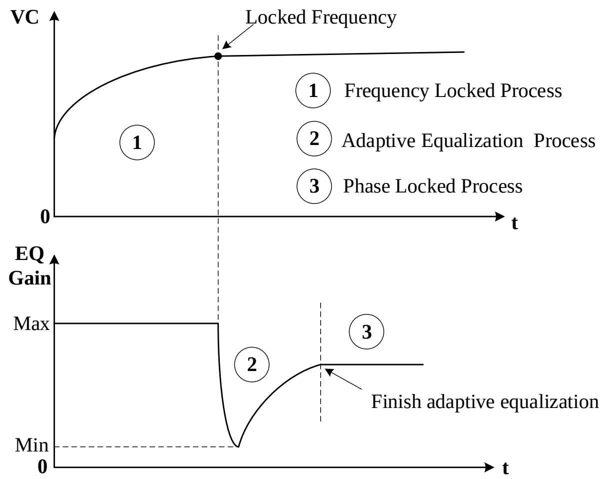



**Figure 2.** *Operation of proposed wireline receiver*

The detailed operation of the proposed receiver is shown in Figure 2. The adaptive EQ and the reference-less CDR are combined in receiver by using three signals: *EQ*, *FD* and *PD*, in which the *FD* and *EQ* signals are generated from the frequency detector circuit, and the *PD* signal is created from the adaptive EQ circuit. The receiver operation is divided into three stages. In the first stage, the switch S2 turns off ($FD$ = 0, $PD$ = 0) and switch S1 turns on ($FD$ = 0, $EQ$ = 1) to activate the frequency acquisition process while the EQ gain of the adaptive EQ is set to a maximum to minimize the effect of the ISI. After that, the FD circuit tracks the frequency error between the incoming data and the output recovery clock to decrease this error. When the frequency error is reduced to a small enough value, the *FD* signal is activated ($FD$ = 1) by the frequency lock detector to make S1 off and S2 on. The frequency locked process finishes and the operation of the receiver turns to the second stage. At this stage, the EQ gain is reset to its minimum value to start the adaptive equalization process. Subsequently, depending on channel condition, the EQ gain increases to compensate the channel loss. When the adaptive equalization process finishes, the EQ gain is fixed, the EQ triggers *PD* signal ($PD$ = 1) to turn the operation of the receiver to next stage. At the final stage, the half-rate binary PD takes over the final phase acquisition process.

## 3. Principle of adaptive equalization and frequency detection in wireline receiver

### *3.1. Adaptive equalization principle of EQ*

The principle of adaptive equalization is demonstrated in Figure 3. The high-speed serial data after passing the channel ($EQ_{IN}$) is sampled by a half-rate clock (CK) by a D-type Flip-Flop (D-FF). Because the data is affected by ISI, the clock will sample the data at the correctly and wrongly logical values (see Figure 3). The number of wrongly logical values is proportional to the effect of the ISI. If the data is heavily influenced by ISI then wrongly logical values will appear more and if the data is less affected by ISI then wrongly logical values will arise rarely when sampling is performed. Thus, data sampling will evaluate the impact of ISI on high-speed serial data. Based on this principle, an 8-bit counter is used to count the number of edges of the data after sampling for adaptive equalization [16].

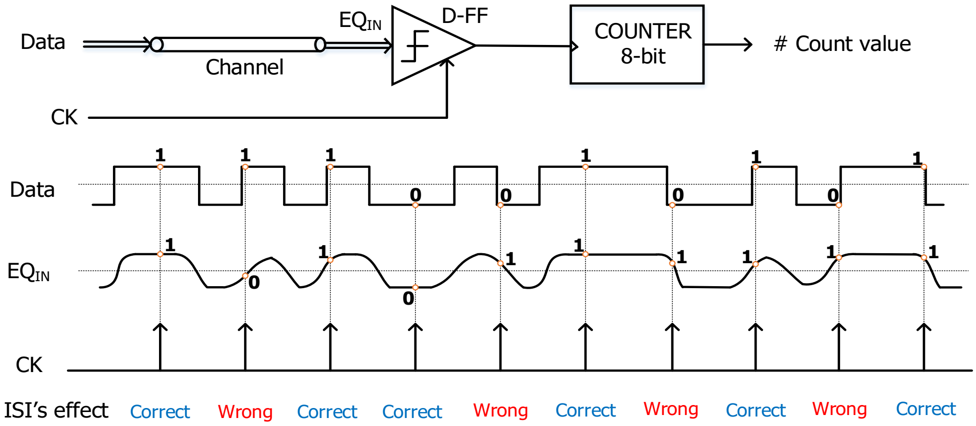



**Figure 3.** *Adaptive equalization principle*

As discussed earlier, adaptive equalization process is started by setting the minimum EQ gain (C[3:0] = 0000) to maximize the effect of ISI. Then, the EQ gain will be gradually increased until the wrongly logical values when sampling is minimized, the digital control code C[3:0] is fixed, and the adaptive equalization process is terminated [16]. As a result, the impact of ISI on high-speed serial data is minimized.

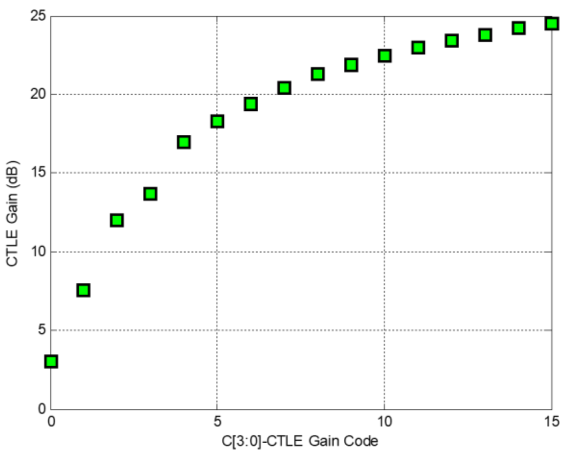



**Figure 4.** *Gain of CTLE*

In this work, we propose using a CTLE to obtain both high boost gain and wide DC gain range for ISI elimination and low power consumption, simultaneously. The CTLE structure based on RC source-degeneration equalizer is implemented with a $2^{nd}$-order negative capacitor circuit

[16]. To achieve a wide compensation range for channel loss, the three-stage CTLE is designed with 16 possible gain values corresponding to control code C[3:0] as shown in Figure 4. The CTLE has an adjustment range of 21.8 dB, from 3 dB to 24.8 dB.

### *3.2. Frequency acquisition principle of reference-less CDR*

The coarse/fine frequency acquisition schemes were introduced in [1] and [2] for a wide-range reference-less CDR. In these proposals, the coarse FD (CFD) and fine FD (FFD) operate dependently, whereby the fine frequency acquisition loop starts just after the coarse frequency tracking loop finishes. Consequently, the CDR has long frequency acquisition time. In this work, the using of coarse/fine frequency acquisition scheme is proposed as well but with simultaneous operating mechanism of the CFD and FFD in frequency tracking process to obtain shorter frequency acquisition time [17].

The CFD block diagram is illustrated in Figure 5. The circuit is composed of a frequency decrement acquisition (Coarse Frequency Dn Control), a frequency increment acquisition (Coarse Frequency Up Control), a D-FF, two OR-gates, and two multiplexers. In this circuit, the signal $DN_F$ and $UP_F$ at the OR-gate inputs are generated by the FFD. Moreover, the *Sel* signal, which is the output of a positive-edge-triggered D-FF is used to control the selection $UP_C/DN_C$ signals at the output of the CFD where $UP_C$ and $DN_C$ are outputs of the frequency increment acquisition circuit and the frequency decrement acquisition circuit, respectively.

Based on the *Sel* signal, the operating principle of the proposed CFD is as follows. If the *Sel* signal is low (the data is slower than the clock), the MUX1 selects $UP_F$ as the output of the CFD ($UF_{FD} = UP_F$) and the MUX2 selects the output of the OR2 as the output of the CFD ($DN_{FD} = DN_C + DN_F$). Because the $DN_{FD}$ signal dominates over $UP_{FD}$ signal in this case, so the CFD operates as if the frequency decrement acquisition process until arising $UP_C$ signal [18]. On the contrary, if the signal *Sel* is high (the data is faster than the clock), the MUX1 selects the output of the OR1 as the output of the CFD ($UP_{FD} = UP_C + UP_F$) and the MUX2 selects $DN_F$ as the output of the CFD ($DN_{FD} = DN_F$). When the FD closes to frequency locked state, $UP_C$ is approximate to zero so the output of the FFD becomes the output of the CFD. The FD remains the FFD in operation. As a result, the proposed architecture allows the CFD and the FFD to operate simultaneously. Thereby, this architecture increases probability that the pulse $UP_{FD}$ and $DN_{FD}$ appear to drop frequency acquisition time.

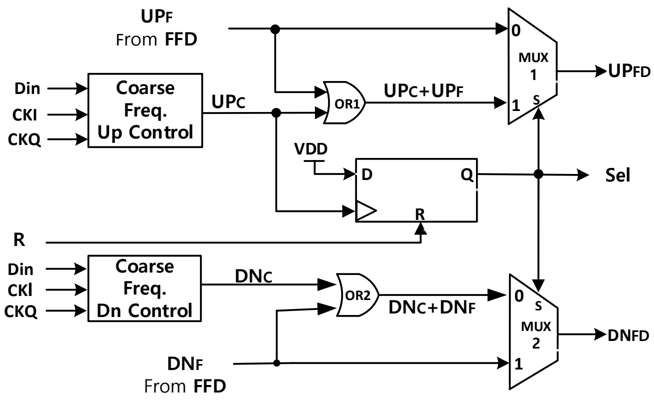



**Figure 5.** *Two-step frequency tracking scheme of the wide-band FD*

Based on the operation principle of the wide-band FD, we design the reference-less CDR with the values of the parameters in the CDR circuit as presented in Table 1. In which, $I_{CP\text{-}FD}$ and $I_{CP\text{-}PD}$ are charge/discharge currents for the frequency tracking loop and the phase tracking loop, respectively. R1, C1 and C2 form $2^{nd}$-order loop filter. A ring-VCO with four-stage [18] is employed to generate frequency from 1.2 GHz to 1.5 GHz.

**Table 1.** *Design parameter values in the CDR*

| | | | | | |
|---|---|---|---|---|---|
| C1 | 2 nF | R1 | 450 Ω | $I_{CP\text{-}FD}$ | 400 µA |
| C2 | 60 pF | $I_{CP\text{-}PD}$ | 20 µA | $F_{VCO}$ | (1.2÷1.5)GHz |

## 4. Simulation results and discussion

A 2.4 to 3 Gb/s reference-less wireline receiver is implemented in a 180 nm CMOS process. The proposed receiver consumes 42.7 mW from 1.8 V supply voltage without PAD while operating at the maximum input data rate of 3 Gb/s. Table 2 presents a detailed power breakdown. In which, the adaptive EQ consumes 29.7% of the overall power whereas the reference-less CDR consumes 57.1% of the overall power at 3 Gb/s.

**Table 2.** *Detailed power breakdown at 3 Gb/s*

| Block | Power |
|---|---|
| EQ | 12.7 mW (29.7%) |
| CDR | 24.4 mW (57.1%) |
| Others | 5.6 mW (13.2%) |
| **Total** | **42.7 mW** |

To verify the adaptive equalization in the proposed receiver, a channel loss model as illustrated in Figure 6 is utilized. The channel has loss of 16.5 dB at 3 Gb/s. A 3 Gb/s PRBS-7 data is applied as input of the receiver. Figure 7 depicts simulation result of equalizer adaptation in the receiver. At the start, the CTLE gain is established to maximum (C[3:0] = 1111). After that, it is set to minimum (C[3:0] = 0000) to start the adaptive equalization process. When *SS* signal arises the control codes C[3:0] are updated to grow the CTLE gain. The equalizer adaptation finishes when *PD* signal appears. The C[3:0] is fixed as 0100 and the CTLE boosting gain achieves 16.8 dB. The adaptive equalization time is approximately 4.4 µs.

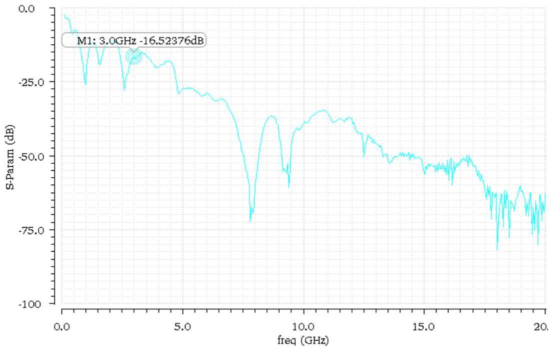



**Figure 6.** *Channel loss model*

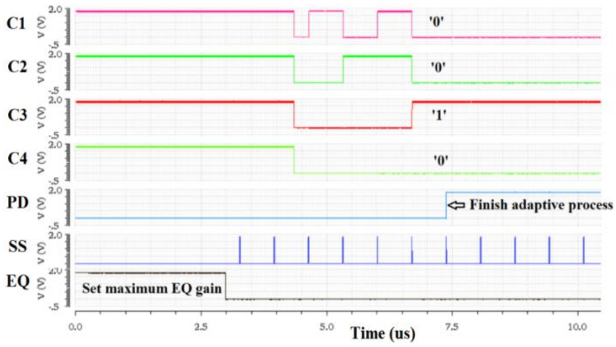



**Figure 7.** *Adaptive process of the EQ in the receiver*

Figure 8 presents operation of the proposed receiver in simulation. The acquisition process of the receiver is divided by three periods. At the start, the frequency acquisition process operates with the initial VCO frequency is 1.2 GHz. As mentioned, the EQ gain is set to maximum in this period to minimize the ISI influence to the frequency tracking process of the receiver. Then, the control voltage (VC) increases to grow the VCO frequency and decrease frequency error between half the data rate and the VCO frequency. When the frequency error is small enough (the VCO frequency closes to 1.5 GHz), the frequency lock detector toggles the signal *FD* to the high state to turn-off the frequency detector. After that, the receiver transfers the loop control to the EQ (period 2). The adaptive equalization process works to compensate the channel loss as above mentioned. When the equalizer adaptation accomplishes, the *PD* signal is activated to turn the loop control to the phase locked process (period 3). The receiver has the frequency tracking time and the acquisition time of 3 µs and 7.4 µs, respectively.

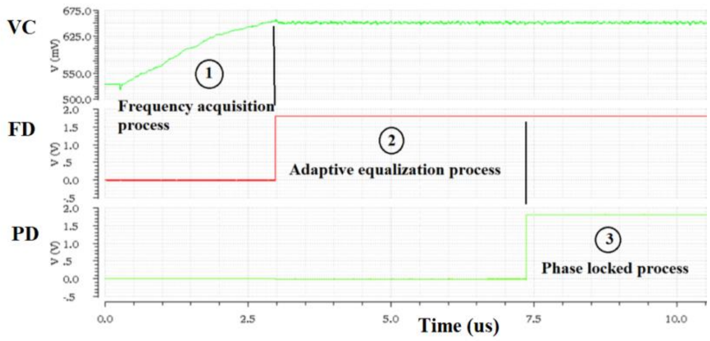



**Figure 8.** *Operation of proposed receiver*

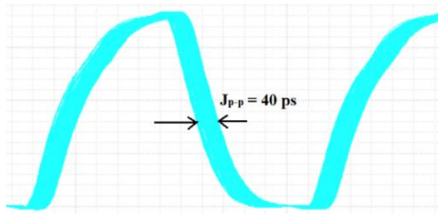
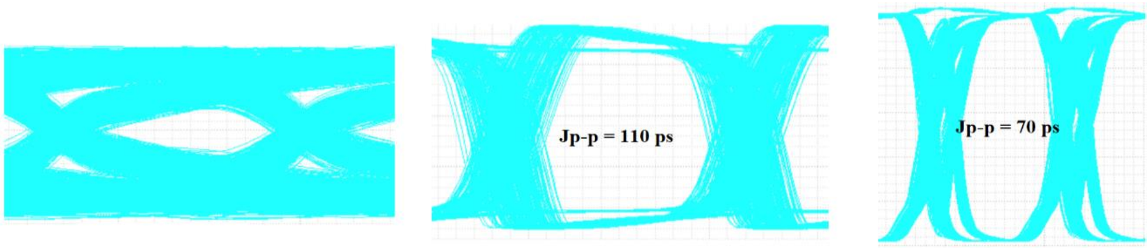



**Figure 9.** *Waveform of recovered clock at 3 Gb/s input data*




(a) (b) (c)

**Figure 10.** *Eye diagram of data: (a) at input, (b) after equalization, (c) after recovery*

Figure 9 and Figure 10 present waveforms of data and recovered clock, respectively, in which the eye diagram of data at input, after equalization and after recovery are shown in Figure 10(a), (b) and (c), respectively. The jitter peak-to-peak of the recovered clock is 40 ps with 3 Gb/s input data. The eye diagram of the 3 Gb/s data is relatively closed after passing through the lossy channel. It is open in both vertical and horizontal after equalization and recovery. The receiver obtains jitter peak-to-peak of data after equalization and recovery of 110 ps and 70 ps, respectively. As a result, the EQ and the reference-less CDR work well to eliminate the ISI and fall BER. Table 3 lists a performance summary of CDR with equalizer in wireline receiver in literature. This work has the shortest acquisition time and comparable dissipation power when compared to [11], [14], [15]. Specifically, the proposed receiver obtains the acquisition time of 7.4 µs while reference [14] and [15] are 10100 µs and 480 µs, respectively. Moreover, in proposed wireline receiver, compared with [14], [15], the EQ has adaptive equalization capability and compared with [11], the CDR has reference-less architecture.

**Table 3.** *Performance Comparison of proposed receiver*

| | **[11] (measure)** | **[14] (measure)** | **[15] (measure)** | **This work (Simulation)** |
|---|---|---|---|---|
| Technology | 28 nm CMOS | 28 nm CMOS | 40 nm CMOS | 180 nm CMOS |
| Supply (V) | 1 | 0.9 | 1.2 | 1.8 |
| Data Rate (Gb/s) | 6 | 22.5-32 | 10.432-16 | 2.4-3 |
| Equalizer | Adaptation | Without adaptation | Without adaptation | Adaptation |
| CDR Architecture | Reference | Reference-less | Reference-less | Reference-less |
| Acquisition Time | N/A | < 10100 µs | < 480 µs | 7.4 µs |
| $[(F_{DATA}-F_{CLK})/F_{CLK}]$ | | [+14.3%] | [+23.8%] | [+25%] |
| Channel Loss (dB) | 27.8 | 14.8 | 10.14 | 16.5 |
| Power (mW) | 31@6Gb/s | 102@32Gb/s | 39.9@16Gb/s | 42.7@3Gb/s |

## 5. Conclusion

The proposed wireline receiver is implemented in 180 nm CMOS process. The wireline receiver has simple architecture and achieves short acquisition time. By using the digital adaptation algorithm based on counter, the EQ obtains both the fast equalizer adaptation time and low power consumption. A two-step frequency tracking scheme and simultaneous operation of the CFD and FFD are employed to fall frequency acquisition time, outperforming previous published wireline receiver. The limitation of this work is that there are no measurement results yet and without decision feedback equalizer (DFE) in equalization process. Therefore, in future work, we will tape out chip to get measured results and integrate the CTLE and DFE in equalization process to further improve the ISI elimination of the wireline receiver.

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