A 551-ns SETTLING TIME OUTPUT CAPACITOR-LESS LDO WITH PROTECTION CIRCUITS

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ABSTRACT

This paper proposes an output-capacitorless low-dropout regulator (OCL-LDO) with simple structure and fast load transient response for system-on-chip applications. The proposed OCL-LDO does not require output capacitance and remains stable at no-load condition. A combining frequency compensation technique is utilized to reduce on-chip compensation capacitor without degrading loop stability at light load and improve load transient response speed simultaneously. In addition, over-temperature, over-voltage, and short-circuit protection functions are also integrated into the OCL-LDO to ensure circuit safety during operation. The proposed OCL-LDO regulator has been implemented and simulated in a 180 nm CMOS process. Simulation results demonstrate the OCL-LDO regulates the output at 0.9 V from a voltage supply of 1.8 V. The protection circuits turn off the OCL-LDO when a problem occurs. The OCL-LDO consumes 71.6 µA quiescent current at light load and can recover within 655 ns for load transient from 0 to 100 mA and within 551 ns for load transient from 100 mA to 0 in 100 ns. The OCL-LDO obtains good load regulation of 2.54 µV/mA.

MẠCH LDO KHÔNG SỬ DỤNG TỤ ĐIỆN NGOÀI CHIP TÍCH HỢP CÁC MẠCH BẢO VỆ CÓ THỜI GIAN KHÔI PHỤC 551 ns

Nguyễn Thành Long
Viện Khoa học và Công nghệ Quân sự

THÔNG TIN BÀI BÁO

Ngày nhận bài: 12/4/2024
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Ngày đăng: 31/5/2024

TỪ KHÓA

Mạch ổn áp
Không sử dụng tụ điện tại đầu ra
Bù tần số
Chức năng bảo vệ
Thời gian khôi phục

TÓM TẮT

Bài báo này đề xuất thiết kế mạch ổn áp điện áp rơi thấp không sử dụng tụ điện tại đầu ra (OCL-LDO) với cấu trúc đơn giản và đáp ứng chuyển tải nhanh cho các ứng dụng tất cả trên một chip. Mạch OCL-LDO đề xuất ổn định trong điều kiện tải nhẹ mà không yêu cầu tụ điện tại đầu ra. Kỹ thuật bù tần số kết hợp được sử dụng để giảm giá trị tụ điện bù trong chip mà không làm giảm sự ổn định của mạch trong khi cải thiện được tốc độ đáp ứng chuyển tải. Bên cạnh đó, các chức năng bảo vệ quá nhiệt, quá dòng, ngắn mạch cũng được tích hợp trong mạch OCL-LDO để đảm bảo mạch an toàn trong suốt thời gian hoạt động. Mạch ổn áp OCL-LDO được thiết kế và mô phỏng trên công nghệ CMOS 180 nm. Kết quả mô phỏng cho thấy mạch OCL-LDO tạo ra điện áp đầu ra ổn định 0,9 V từ điện áp nguồn cung cấp 1,8 V. Mạch bảo vệ tắt mạch OCL-LDO khi có sự cố xảy ra. Mạch OCL-LDO tiêu thụ 71,6 µA dòng tĩnh trong điều kiện tải nhẹ và có thể khôi phục điện áp đầu ra trong 655 ns khi dòng tải thay đổi từ 0 đến 100 mA và trong 551 ns khi dòng tải thay đổi từ 100 mA về 0 trong 100 ns. Mạch OCL-LDO đạt được điều chỉnh tải tốt với 2,54 µV/mA.

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1. Introduction

The power management ICs are critical modules in today's system-on-chip Internet-of-Things, and mobile devices applications. Various types of power management units are required for widely distributed voltage domains [1]. Low-dropout regulators (LDO) are usually cascaded after power-efficient switching regulators to filter the switching ripples and provides a regulated supply voltage [2]. However, excess loading current output, improperly shorting output terminals, or over temperature will possibly damage the LDO regulator. As a result, design of LDO is necessary to integrate internal protection functions to improve the stability and safety. So far there are several researches about protection circuits for LDO [3] – [7]. In which, researches [3], [4] present principle of current protection, paper [5] illustrates solution to protect voltage and over-temperature, and researches [6], [7] show architecture of over-temperature and current protection circuits. However, these studies only focused on the design of protection circuits without carefully evaluating the quality of LDO circuit when integrated with protection circuits.

Conventional LDOs have an off-chip capacitor in the order of several micro-farads at the output to stabilize the system [8]. However, using bulky off-chip output capacitors for stability and the power supply rejection ratio (PSRR) significantly affects the system size. Output capacitor-less LDO (OCL-LDO) is beneficial to reduce its area and increase the integration density by removing a bulky external capacitor [9], [10]. However, after getting rid of the large off-chip capacitor, the pole at the LEO output is no longer dominant and the stability control becomes more challenging. To overcome this problem, different compensation techniques using small capacitors (~pF) have been proposed for OCL-LDOs [11] – [18]. Researches [11], [12] utilize internal Miller compensation technique to obtain good phase margin (PM) but they have narrow Gain-Bandwidth (GBW). To improve GBW, researches [13], [14] compensate frequency by combining capacitor and feedback resistor. Unfortunately, they have poor PM. Researches [15], [16] use active feedback technique, paper [17] employs feedforward path compensation and paper [18] utilizes hybrid passive-active frequency compensation to achieve high PM and large GBM simultaneously. However, they have long settling time (T_S), 9 µs in [15], 3.2 µs in [16], 2.2 µs in [17] and 2.6 µs in [18]. To overcome these limitations, research [19] combines internal Miller compensation, combining capacitor and feedback resistor, and active feedback. It obtains a short settling time of 0.59 µs. However, these studies have not integrated the protection function in the LDO circuit.

This paper proposes a OCL-LDO integrating protection circuits inside, including over-voltage, short-circuit and over-temperature protection. In addition, by using the frequency compensation technique in [19], the proposed OCL-LCO achieves short settling time. This paper is organized as follows. Section 2 introduces the detailed design of the the proposed OCL-LDO. Section 3 shows the experimental results on 180 nm CMOS process followed by conclusions in Section 4.

2. Design of proposed OCL-LDO

2.1. Frequency compensation technique for OCL-LDO [19]

Figure 1 describes the change in output voltage V_{OUT} of OCL-LCO when the load current I_{load} changes from low (I_L) to high (I_H) in two cases GBW_1 and GBW_2 [20].

When the GBW_1 is larger than the GBW_2, the T_S in case of GBW_1 is shorter than that of GBW_2. As a result, GBW is inversely proportional to the T_S. As mentioned in [11], the Miller capacitor (C_C) is inversely proportional to the GBW of the system, increasing the C_C value will decrease the GBW value, leading to an increase of T_S. Therefore, to reduce T_S when the load current changes, we can rise GBW or fall the C_C capacitor value. However, the decreasing C_C means reducing circuit stability. To deal with this problem, research [19] proposed a frequency compensation architecture as shown in Figure 2.

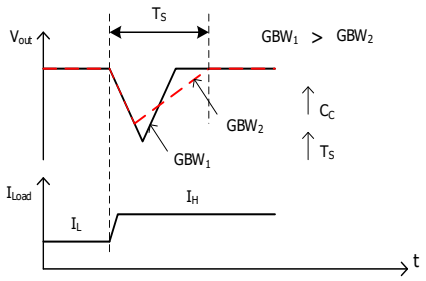


Figure 1. *The block diagram of proposed wireline receiver*

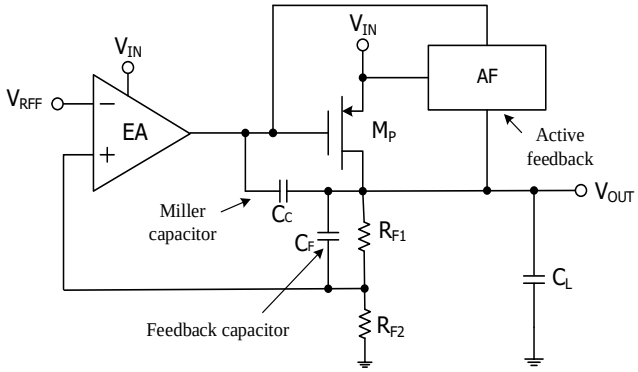


Figure 2. *Frequency compensation technique for OCL-LDO*

By using three compensation methods simultaneously: internal Miller capacitor, combining capacitor and feedback resistor, and active feedback, this proposal achieves high DC gain (> 90 dB), good PM (> 60^0) to ensure stable operation for OCL-LDO while improving GBW. As a result, the T_S decreases. The designed values of capacitors and resistors in OCL-LDO core circuit are shown in Table 1.

Table 1. *Designed parameters of OCL-LDO core circuit*

Parameter	Value
C_C	5.9 pF
C_F	4.5 pF
C_L	10 pF
R_{F1}	8 kΩ
R_{F2}	16 kΩ

2.2. Design of protection circuits for OCL-LDO

2.2.1. Design of short-circuit protection circuit

As it has already being mentioned, the LDO output voltage is regulated meaning that it is constant. If a short-circuit exists, the output voltage will drop to a very low value or even to zero, suddenly. The protection circuit has to be able to sense these voltage changes, sharply, and produce a control signal that will tum off the LDO. Thus, the short-circuit protection circuit protects the LDO from a short-circuit issue on the output, improving the reliability and stability of the system. The operation principle of short-circuit is illustrated in Figure 3.

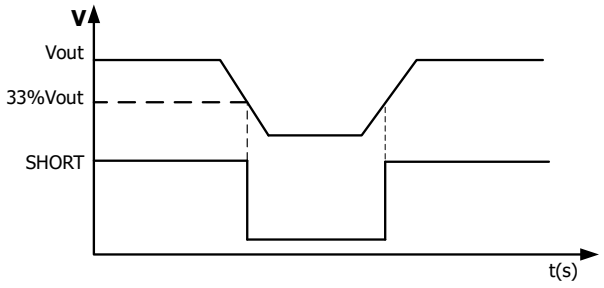


Figure 3. *Short-circuit protection principle*

Short-circuit protection circuit is designed based on a comparator circuit. The comparator will compare two input signals including an LDO output voltage and a reference voltage. When a short-circuit issue occurs, the output voltage of the LDO drops suddenly and goes through a threshold that is 33% output voltage in this paper, then the output signal of the circuit (SHORT) goes to low logic to turn off the LDO. When the LDO circuit output voltage increases to greater

than 33% its desired output voltage, the SHORT signal becomes high logic to indicate that the short-circuit issue has ended.

2.2.2. Design of over-voltage protection circuit

LDO provides stable output voltage, ensuring reliable operation of electronic devices. However, in some cases the output voltage of the LDO increases suddenly, which can damage the electronic devices powered by the LDO. Therefore, integrating an over-voltage protection circuit (OVP) in the LDO is very important to limit the output voltage within a safe threshold and avoid unwanted situations. The design of over-voltage circuit is based on a comparator circuit similar to the short-circuit protection circuit. When the output voltage exceeds the safe threshold, the protection circuit will be activated to turn-off the LDO. The LDO will be activated again when the output voltage returns the safe operation range. Figure 4 demonstrates principle of OVP circuits.

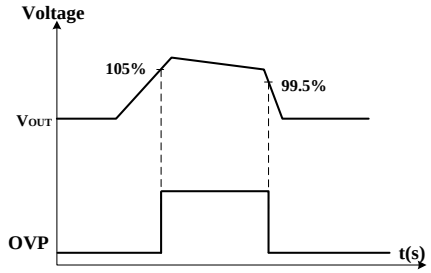


Figure 4. *Over-voltage protection principle*

In this paper, the upper thresholds is selected as 105% output voltage. When the output voltage exceeds 105% its expected value, the LDO will be turned off (OVP signal stays in high logic), next when the output voltage reaches 99.5%, the protection circuit will turn on the LDO again (OVP signal stays in low logic).

2.2.3. Design of over-temperature protection circuit

During chip operation, with an increase in ambient temperature or heat accumulation inside the chip, the temperature inside the chip will keep increasing. Furthermore, the essence of LDO is to regulate voltage by changing the resistance in the power transistor. So if the input and output voltages are not equal, all the remaining power will be dissipated as heat in the LDO. This heat can be significant if we use such a regulator for high load currents. In addition, when the circuit operates, the power transistor usually has a large size, large current consumption, and large resistance, so the amount of heat emitted through it is also large. After several periods of operation, the circuit temperature gradually increases. If too much heat is dissipated without intervention to reduce the temperature effect on the device, the device may shut down. As a result, it can reduce the device's life-span. To protect the chip from damage, an overheating protection circuit (TSD) is designed and widely used in the chip. Figure 5 presents change characteristics of over-temperature protection circuit.

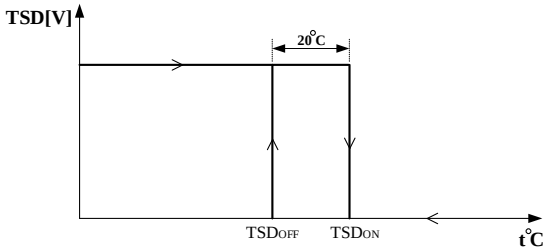


Figure 5. *Temperature change characteristics of over-temperature protection circuit*

When the internal temperature of the LDO reaches to the design value of the overheat protection (140^0C in this design), the overheat protection function will activate (TSD_{ON}) to turn-off the LDO. After that, the internal temperature starts to drop when the temperature delay function is activated, meaning the overheat protection circuit stops working (TSD_{OFF}) until the temperature drops 20^0C compared to the LDO turn-off temperature.

The circuit is designed based on the voltage comparison between the (+) and (-) terminal of the operational amplifier (OPA) circuit as shown in Figure 6. At the anode of the comparator circuit, a PNP bipolar transistor is connected to detect the temperature change. At the cathode, the reference voltage is applied to the overheat protection circuit through a voltage divider.

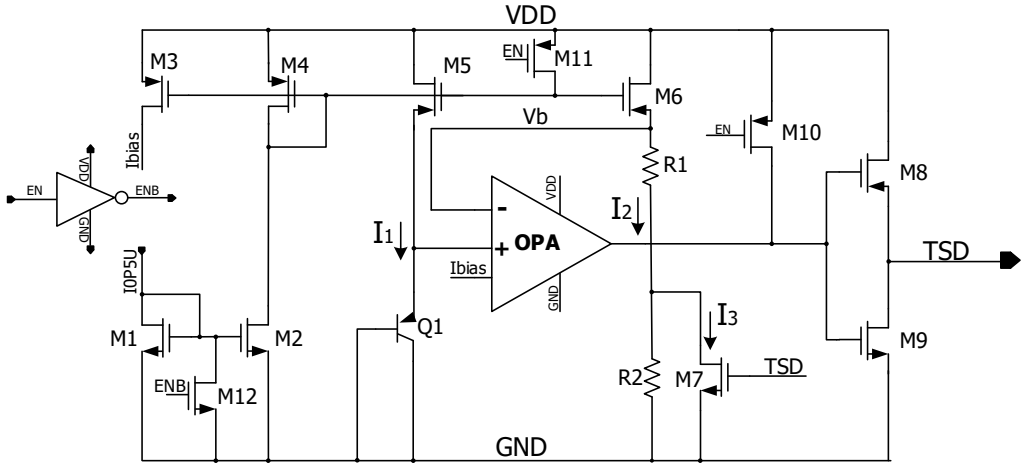


Figure 6. *Schematic of over-temperature circuit*

The comparator circuit (OPA) is used to compare the voltage produced by the constant current I_2 and the voltage change caused by the temperature-dependent current I_1. The temperature-dependent current is generated by a diode-connected transistor Q1 for absolute temperature. When temperature increases, the voltage at anode of the OPA grows as well. Since it becomes larger than the voltage at the cathode, the OPA will generate a high logic signal which passes through an inverter (M8, M9) to generate a low logic signal (TSD). This signal is applied to the OCL-LDO core circuit to turn-off the LDO. The shutdown and reset temperatures T_1 and T_2 respectively are calculated using the formulas [5]:

$$T_1 = \frac{\left[(R_1 + R_2)I_2 - I_3R_2\right]q}{k\ln(\frac{I_1}{I_{EBS1}})} \quad (1)$$

$$T_2 = \frac{(R_1 + R_2)I_2q}{k\ln(\frac{I_1}{I_{EBS2}})} \quad (2)$$

In which, R_2 and R_3 are resistors that create a constant current I_2; I_3 is the drain current of M7; I_1 is the temperature dependent current; q is the electron charge; k is Boltzmann's constant; I_{EBS1} and I_{EBS2} are the emitter–base currents at temperatures T_1 and T_2, respectively. Equations 1 and 2 reveal that, R2, R3 are adjusted to vary the on/off temperature threshold of TSD circuit.

2.3. Integrating protection circuits into OCL-LDO core circuit

Solution integrating protection circuits into OCL-LDO core circuit is demonstrated in Figure 7. The circuit consists of an NOT gate, a three-input AND gate and a PMOS transistor.

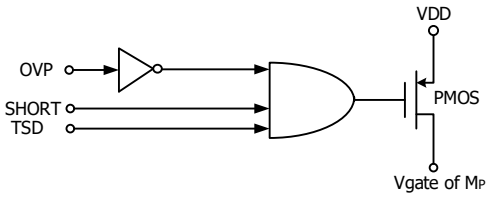


Figure 7. *Integrating protection circuits into OCL-LDO core circuit*

The SHORT, TSD and $\overline{OVP}$ signals are applied the three-input AND gate to drive Gate terminal of the PMOS transistor. When a problem occurs (over-voltage (OVP = 1) or short-circuit (SHORT = 0) or over-temperature (TSD = 0)), a low logic level is put on Gate terminal of the PMOS transistor to turn-on PMOS. Then, Drain terminal of PMOS transistor which connects to V_{gate} of power transistor in the OCL-LDO core circuit (see Figure 2) is pulled up to VDD. As a result, the OCL-LDO is turned off.

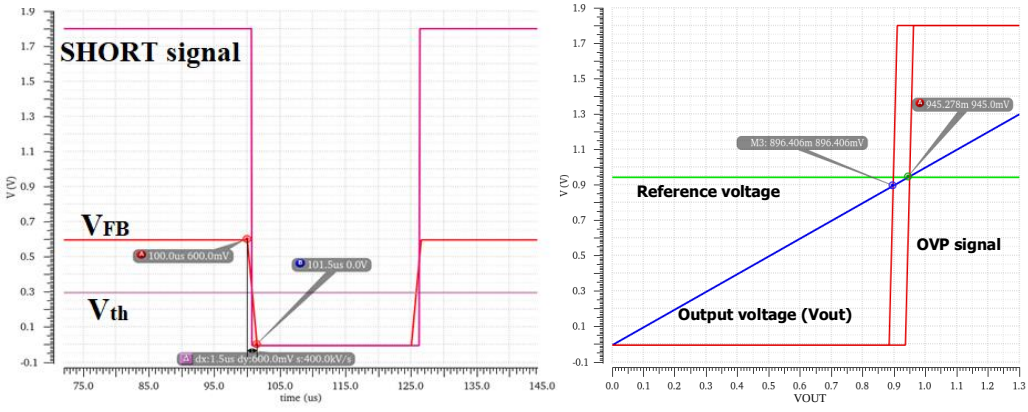
3. Simulation Results and Discussion

A OCL-LDO including protection circuits is implemented in a 180 nm CMOS process. In this design, the input voltage range of the OCL-LDO varies from 1.6 to 2 V and the output voltage of the proposed OCL-LDO is regulated at 0.9 V. The proposed OCL-LDO consumes 128.88 µW from 1.8 V supply voltage. Detailed power breakdown of proposed OCL-LDO is presented in Table 2.

Table 2. *Detailed power breakdown of proposed OCL-LDO*

Block	Power
OCL-LCO core	115.2 µW
OVP	2.25 µW
SHORT	3.94 µW
TSD	7.49 µW
Total	**128.88 µW**

Simulation results of the short-circuit, over-voltage and over-temperature protection circuits are illustrated in Figure 8a, Figure 8b, Figure 9, respectively. The short circuit event is simulated by a sudden decrease (0.6 V to 0 V) in the feedback voltage (V_{FB}) of the LDO during 1.5 µs. The protection circuit is activated when V_{FB} is about 300 mV to change SHORT signal from high to low logic level to turn-off the OCL-LDO.



(a) *(b)*

Figure 8. *Simulation result of (a) the short-circuit and (b) over-voltage protection circuit in the OCL-LDO*

The output voltage (V_{out}) is ramped from 0 to 1.0 V to create over-voltage event and the OVP signal is monitored. When V_{out} exceeds 105% its expected value (945 mV), the OVP signal is

triggered (over-temperature circuit works) to turn-off the OCL-LDO and when V_{out} decrease to 99.5% its expected value (896.4 mV), the OVP signal varies from high to low (over-temperature circuit stops working) to turn-on the OCL-LDO again.

The voltage at cathode terminal of OPA is proportional to temperature. It exceeds voltage at the anode terminal when the temperature is greater than 140^0C. Then, the over-temperature circuit is activated to turn-off the OCL-LDO (TSD signal varies from high to low). After that, when the temperature decreases to 120^0C, TSD signal changes from low to high to turn-on the OCL-LDO again. The simulation results in Figure 8 and Figure 9 present that proposed protection circuits operate well, turn-off the OCL-LDO when a problem such as temperature or voltage occurs.

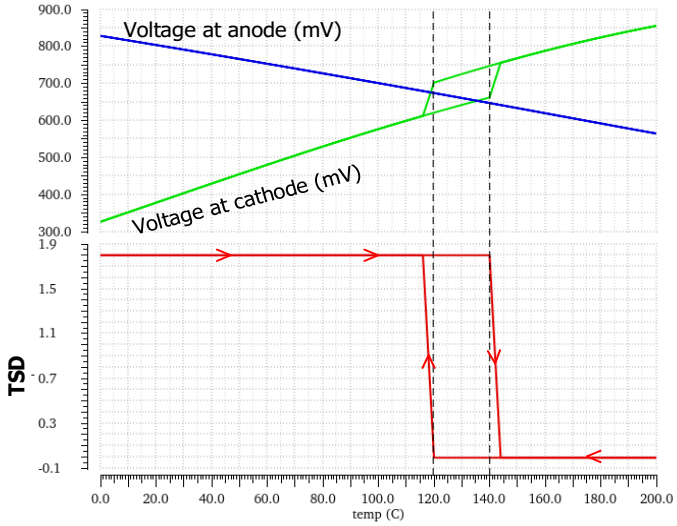


Figure 9. *Simulation result of the over-temperature protection circuit in the OCL-LDO*

The load regulations of the proposed OCL-LDO for supply voltage of 1.8 V is shown in Figure 10. The maximum variation of output voltage V_{out} is 0.254 mV for load current I_{load} change from 0 - 100 mA. Figure 11 demonstrates simulation result of the output voltage change with temperature. The maximum variation of V_{out} is 0.825 mV for temperature variation from -40^0C – 125^0C.

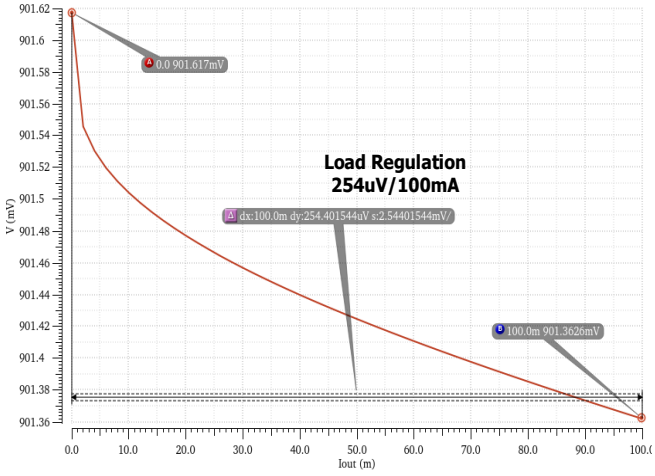


Figure 10. *Load regulation of the proposed OCL-LDO*

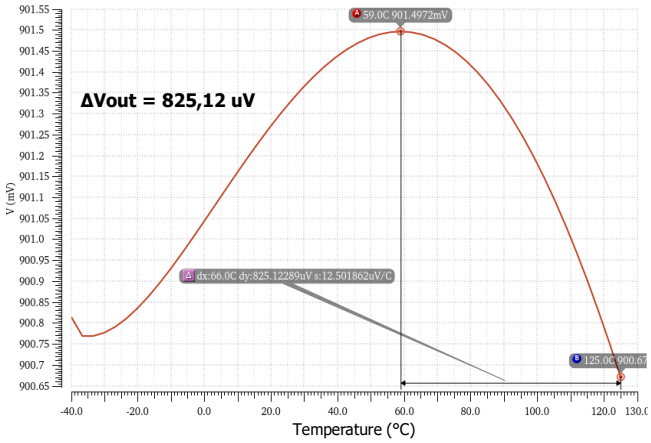


Figure 11. *Variation of output voltage with temperature*

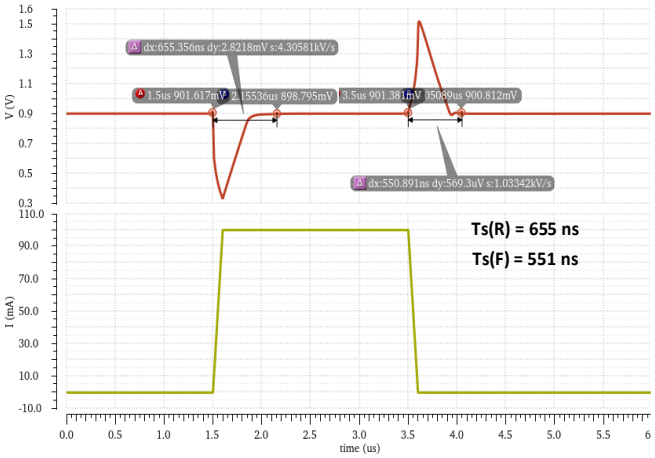


Figure 12. *Load transient response*

Table 3. *Performance comparison of proposed OCL-LDO*

	[11] (simulation)	**[16] (measure)**	**[17] (measure)**	**[18] (measure)**	**This work (simulation)**
Technology	180 nm CMOS	65 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm CMOS
Supply (V)	3.3	1.2	1.8	1.8	1.8
Output voltage (V)	1.8	0.8	1.0	1.2	0.9
Quiescent current (µA)	100	14	6.9	380	71.6
$I_{L,\,max}$ (mA)	50	100	100	100	100
$I_{L,\,min}$ (µA)	0	0	0	0	0
T_{edge} (ns)	N/A	220	100	50	100
Load regulation (mV/mA)	1.36	0.09	0.01	N/A	0.00254
Settling time T_S (µs)	21.85	3.2	2.2	2.6	0.55
Including protection function	No	No	No	No	Yes

Figure 12 shows the transition response when I_{load} change from 0 to 100 mA with 100 ns transition edge times (t_{edge}), the settling time is 0.655 µs. On the other hand when I_{load} change from 100 mA to 0, the settling time is 0.551 µs. Table 3 lists a performance summary of OCL-LDO. This work has the shortest settling time and comparable dissipation power when compared to [11], [16]-[18]. Specifically, the proposed OCL-LDO obtains the settling time of 0.55 µs while references [11], [16], [17] and [18] are 21.85 µs, 3.2 µs, 2.2 µs and 2.6 µs, respectively.

Moreover, the proposed OCL-LDO involves the protection circuits to ensure safety for LDO during work.

4. Conclusion

A fast-transient output-capless LDO including protection function is proposed in this paper. Combining frequency compensation technique reduces compensation capacitor, enhances GBW and increase response speed as well. The experimental results verify that compared to other OCL-LDOs, circuit performance is obviously improved, including shorter settling time as well as good load regulation. The limitation of this work is that there are no measurement results yet and the power consumption is quite high. Therefore, in future work, we will tape out chip to get measured results and optimize the circuit to reduce current consumption.

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